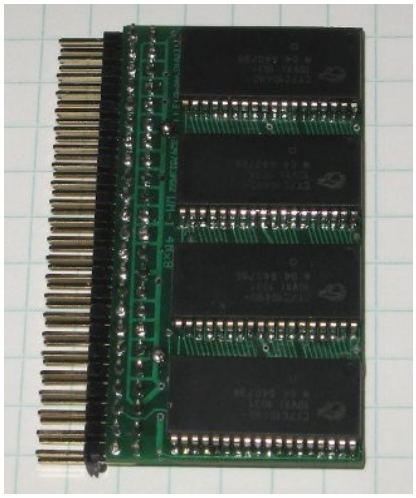
WM-1 32Mb 4Mx8 5V SRAM Module



- easiest RAM type to implement in homebrew computers
- eight 10ns ISSI IS61C5128AL-10KLI 512Kx8 5V SRAMs, four on each side. See ISSI data sheet at http://www.issi.com/WW/pdf/61-64C5128AL.pdf . Keep the total capacitive bus loading in mind when calculating what actual speed performance will be. TTL-level I/O, which is no problem for a 65816 processor using the typical 74ACT245 data-bus transceiver.
- six embedded (for minimum inductance) .1µF bypass capacitors
- four ground pins and two Vcc pins, distributed so no signal pin is more than .2" away from a ground or bypassed Vcc pin
- eight separate CE\ pins, possibly allowing faster selects by handling the computer's entire address-decoding scheme with programmable logic if desired than you would get from adding a 74xx138 to this plus the computer's other address-decoding logic
- two WE\ pins, one for each set of four ICs, so your circuit can write-protect half at a time if desired
- two OE\ pins, one for each set of four ICs (grouped the same way as the WE\ pins)
- two-layer board's high-speed performance is maximized by unorthodox layout and bypass chip capacitors under the ICs actually embedded in the board for minimum inductance
- 46-pin dual-row header of .025" square posts on .100" or optional .300" centers, to plug into readily available, inexpensive thru-hole sockets on your prototyping boards (I can supply the sockets too)
- symmetrical pin-out lets you plug it in backwards and it will still work! (This is possible with SRAM because as long as data lines go do data pins, it doesn't matter if they get mixed up; the same goes for address lines, and the same goes for CE\ lines. I have also done this with EPROM to make the board easier to route, and then used a programming adapter.)
- 2.300" long x 1.234" wide, not including connector
- available with straight or 90° pins & .100" row spacing, or 90° pins & .300" row spacing (Specify.)
- Partial assemblies in half-megabyte increments are available for lower prices, using the same board. Even if you order only one or two ICs on the board, one advantage to you may be the easier, faster assembly of your computer because of the pin header (ie, not having to solder with SMT-only devices), be able to build it on perfboard (although for high-speed applications I still recommend using at least a ground plane on one side like Twin Industries' 8100-series protoboards (http://twinind.com/index.php/products/prototyping-boards/8100-series-plated-through-holes-single-powerground-plane) if not also a Vcc plane on the other side like Twin Industries' 8200-series protoboards (http://twinind.com/index.php/products/prototyping-boards/8200-series-plated-through-holes-dual-powerground-plane) and keep parts as close together as possible and wire-wrap wires as short and straight as possible without straining them.)

Note that the ISSI data sheet says 50mA is the maximum current at the maximum speed and 100% duty cycle, a condition that will be rare on the home-built computers this is intended for. Even then, it will be for the one SRAM chip that is active at a time, while the other seven are in standby. All eight will be in standby in those cycles in which I/O or anything else in the memory map is being accessed.

Testing of completed modules involves functional testing of every one of the 4,194,304 addresses of every module.

The pinout is as follows. You'll notice the address-line numbering starts at pin 1 and goes toward the middle for the first half of the address lines, then resumes at pin 46 and continues counting up toward the middle. The same goes for the data lines, and the chip enables. Remember however that you can mix up address lines, and you can mix up data lines, if it makes your layout easier. (Any given address line does not go to the same address pin on all ICs anyway, so some will be mixed up regardless, and the same goes for data lines.) The OE0\ and and WE0\ lines correspond to CE0\ through CE3\, and inside of that, you can mix up CE0\ through CE3\ if the top half of the board is fully populated. The same goes for OE1\ and WE1\ going to the SRAMs on the other end of the board selected with CE4\ through CE7\, so within those four, you can mix up the CE's also if the bottom half of the board is fully populated. If you just tie the OE0\ and OE1\ lines together and the WE0\ and WE1\ lines together, then there are no limitations for mixing up CE\ lines. The A18 line has two pins to make things symmetrical. (You could consider it A4 or anything else you want—it doesn't matter either, except to know that there are two of that one, whatever you decide to call it on your computer board.) These two pins are connected together on the board, so it is not mandatory that you connect both on your layout.

Holding the module as shown on page 3, with the pin header along the left edge and away from you (ie, under the board), such that you see the "WM-1 4Mx8" label in the copper at the left end of U2 and U3, and you see the traces between the ICs going more-or-less parallel to the length of the board and more-or-less perpendicular to the ICs (instead of vice-versa), and the printing on the ICs is upside down, pin 1 of the pin header is on the top left (near the corner of the board), 2 is to its right and .100" farther from the corner of the board. The pin header then comes off the back of the board instead of the front, so the pin-out of the socket on your motherboard is the same as shown below, and is <u>not</u> reversed, either for straight pins or 90° pins on the module.

```
pin 1  A0   □ □  A1  pin 2
       A2   □ □  A3
       gnd  □ □  CE0\
       A4   □ □  A5
       CE1\ □ □  A6
       CE2\ □ □  +5V
       D0   □ □  A7
       A8   □ □  D1
       OE0\ □ □  A18  (dup)
       gnd  □ □  WE0\
       D2   □ □  D3
       CE3\ □ □  CE7\   (middle, axis of symmetry)
       D7   □ □  D6
       WE1\ □ □  gnd
(dup)  A18  □ □  OE1\
       D5   □ □  A17
       A16  □ □  D4
       +5V  □ □  CE6\
       A15  □ □  CE5\
       A14  □ □  A13
       CE4\ □ □  gnd
       A12  □ □  A11
pin 45 A10  □ □  A9  pin 46
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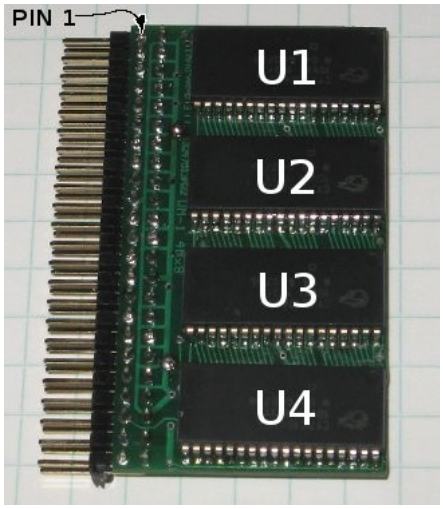
Again, note that pins 18 and 29 (the two A18 pins) are connected together on the board.

The first four IC numbers are shown in the picture at the right. For U5 to U8, the numbering goes around the bottom edge and up the back; so U5 is directly opposite U4, U6 is opposite U3, U7 is opposite U2, and U8 is opposite U1.



For ordering non-fully-populated versions, or for designing your board for one, keep the following in mind:

- U1 is on CE0\, OE0\, and WE0\.
- U2 is on CE2\, OE0\, and WE0\.
- U3 is on CE7\, OE1\, and WE1\.
- U4 is on CE5\, OE1\, and WE1\.
- U5 is on CE4\, OE1\, and WE1\.
- U6 is on CE6\, OE1\, and WE1\.
- U7 is on CE3\, OE0\, and WE0\.
- U8 is on CE1\, OE0\, and WE0\.

So OE0\ and WE0\ go to the four ICs on the top end of the module, and OE1\ and WE1\ go to the four ICs on the bottom end of the module.

As with all CMOS parts, the ICs on the memory module are static-sensitive. Please observe ESD handling precautions. For more information, see: http://ics.nxp.com/packaging/handbook/pdf/pkgchapter3.pdf or http://www.zarlink.com/zarlink/esd-appnote.pdf or do a web search for "electrostatic discharge" or "ESD handling precautions". You will get tons of results. Many of the handling measures may seem extreme and even cost-prohibitive for a private individual to do his own construction. It is possible to handle ESD-sensitive parts without going to extreme lengths *if you understand what does the damage and constantly keep it in mind* as you handle the parts. For equipment, consider a grounded anti-static mat on the workbench to be a minimum, and keep skin (like a bare forearm) in contact with the mat at all times while handling static-sensitive parts. For minimal cost, an anti-static wrist strap (connected to something grounded of course) goes a long way, removing the requirement to always be in contact with the mat to discharge static.

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Updated Apr 23, 2020, for the change from Cypress ICs to ISSI.